Amendments to the Claims

1. (Currently Amended) An arrangement for testing an integrated circuit ~~(1; 21)~~, the arrangement ~~having~~ comprising a data word generator ~~(2; 22)~~, which supplies deterministic data words, ~~having~~ means ~~(3, 4, 5, 6; 22, 23, 24, 25, 26, 27)~~ for test pattern generation, which modify the deterministic data words such that prescribed, deterministic test patterns which can be fed to inputs of ~~an~~ the integrated circuit ~~(1; 21)~~ to be tested, are produced, and ~~having~~ comparison means ~~(12; 30)~~ for comparing test output patterns of the integrated circuit ~~(1; 21)~~ with at least one desired output pattern, the arrangement being provided outside the integrated circuit ~~(1; 21)~~ to be tested.

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2. (Currently Amended) The arrangement as claimed in claim 1, wherein a feedback shift register is provided as ~~a~~ the data word generator ~~(2; 22)~~.

3. (Currently Amended) The arrangement as claimed in claim 1, wherein provided as means ~~(3, 4, 5, 6; 22, 23, 24, 25, 26, 27)~~ for test pattern generation is a bit flipping controller ~~(6; 27)~~ which controls bit flipping logic circuits ~~(3, 4, 5; 23, 24, 25, 26,)~~ such that the deterministic data words are modified in a bitwise fashion such that the prescribed, deterministic test patterns are produced.

4. (Currently Amended) The arrangement as claimed in claim 1, wherein there is provided a masking logic circuit ~~(13; 29)~~ the effect of which is that the comparison means ~~(12; 30)~~ exclusively compare prescribed test output patterns of the integrated circuit ~~(1; 21)~~ to be tested with the desired output patterns.

5. (Currently Amended) The arrangement as claimed in claim 3, wherein a test pattern counter ~~(14; 28)~~ is provided which counts a clock signal and supplies the counting result to the bit flipping controller ~~(6; 27)~~ and/or the masking logic circuit ~~(13; 29)~~.

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6. (Currently Amended) The arrangement as claimed in claim 1, wherein a signature register ~~(30)~~ is provided which logically intercombines consecutive test output patterns, and whose final combination result is compared with a desired output pattern.

7. (Currently Amended) The arrangement as claimed in claim 1, wherein the desired output pattern is generated by means of the data word generator ~~(2)~~ and the ~~with [sic]~~ means ~~(3, 4, 5, 6)~~ for test pattern generation.

8. (Original) The arrangement as claimed in claim 1, wherein the arrangement is implemented as a programmable logic circuit.

9. (Currently Amended) The arrangement as claimed in claim 1, wherein the arrangement is provided on a test board ~~(35)~~ which is connected between a test system ~~(23)~~ and the ~~IC~~ integrated circuit to be tested.

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10. (Currently Amended) A method for testing an integrated circuit ~~(1; 21)~~, in which method deterministic data words are modified such that prescribed, deterministic test patterns are produced which can be fed to inputs of ~~an~~ the integrated circuit ~~(1; 21)~~ to be tested, test output patterns of the integrated circuit ~~(1; 21)~~ to be tested being compared with at least one desired output pattern, and the method being carried out outside the integrated circuit ~~(1; 21)~~ to be tested.